a signal from the means for signalling any one of the components with the clock of the destination component.

6. A computer system as claimed in claim 4 in which the multiplexor comprises an AND gate, and means for transferring gated clock signals from each of the components as inputs to the AND gate.

7. A computer as claimed in claim 6 in which the means for transferring gated clock signals from each of the components as inputs to the AND gate comprises a plurality of OR gates, each such OR gate connected to receive a clock and a gating signal for transferring the clock from one of the components.

8. A computer system comprising:

a first component;

a first clock coupled to said first component, said first component operated in response to timing of said first clock;

a buffer coupled to said first component, said first component always using said first clock to transfer data from said first component to said buffer without synchronizing said transfer of said data to another clock;

a second component coupled to said buffer;

a second clock coupled to said second component, the timing of said first clock being independent of the timing of said second clock, said second component reading said data from said buffer using said second clock without synchronizing said reading to another clock and without transferring other data into said buffer;

a multiplexor coupled to said first component and said second component, said multiplexor receiving a signal from the second component for furnishing a second clock signal from said second clock to said buffer to transfer data to said second component.

9. A computer system as in claim 8 further comprising:

a third component;

a third clock coupled to said third component, said third component operated in response to timing of said third clock, the timing of said third clock being independent of the timing of said first clock,

wherein said first component uses said first clock to transfer further data from said first component to said buffer without synchronizing said transfer of said further data to another clock, and

wherein said third component transfers said further data from said buffer using said third clock without synchronizing said transfer of said further data to another clock.

10. A computer system as in claim 8 further comprising:

a third component;

a third clock coupled to said third component, said third component operated in response to timing of said third clock the timing of said third clock being independent of the timing of said second clock,

wherein said second component uses said second clock to transfer further data from said second component to said buffer without synchronizing said transfer of said further data to another clock, and

wherein said third component transfers said further data from said buffer using said third clock without synchronizing said transfer of said further data to another clock.

11. A computer system as in claim 8 wherein said data may be immediately utilized by said second component without storing said data in said second component.

12. A computer system as in claim 9 wherein said further data may be immediately utilized by said third component without storing said further data in said third component.

13. A computer system as in claim 8 wherein the transfer of said data into said buffer is controlled entirely by said first component and said first clock.

14. A method for transferring data between a plurality of components in a computer system including a first and a second component, said method comprising:

operating said first component using a first clock having a first timing;

operating said second component using a second clock having a second timing independent of said first timing;

transferring an entire packet of data having a plurality of words from said first component to a buffer always using said first clock without synchronizing any of said plurality of words to another clock;

once said entire packet of data is transferred from said first component to said buffer, signaling said second component that said entire packet of data is ready to be transferred to said second component;

transferring said entire packet of data to said second component using said second clock without transferring other data into said buffer;

furnishing a clock signal to said buffer from a multiplexor, said multiplexor coupled to said first component and said second component, said multiplexor receiving a signal from the second component for furnishing a second clock signal from said second clock to said buffer to transfer data to said second component.

15. A method for transferring data as in claim 14, wherein said computer system comprises a third component and wherein said method further comprises:

operating said third component using a third clock having a third timing independent of said first clock;

transferring a further entire packet of data having a second plurality of words from said first component to said buffer using said first clock without synchronizing any of said second plurality of words to another clock;

once said further packet of data is transferred from said first component to said buffer, signaling said third component that said further entire packet of data is ready to be transferred to said third component;

transferring said further entire packet of data to said third component using said third clock without synchronizing any of said second plurality of words to another clock.

16. A method as in claim 14 wherein said second component uses said entire packet of data immediately without first storing said entire packet of data in said second component.

17. A method as in claim 15 wherein said third component uses said further entire packet of data immediately without first storing said further entire packet of data in said third component.

18. A method as in claim 15 wherein said step of signaling said second component occurs by broadcasting a first signal from said first component to said second and third components, said first signal being synchronized to said second clock, and wherein said step of signaling said third component occurs by broadcasting a second signal from said first component to said second and third components, said second signal being synchronized to said third clock.

19. A computer system as in claim 8 further comprising:

a bus for carrying a first signal, said bus being coupled to said first component and said second component, said

first signal being provided by said first component and being synchronized to said second clock, said first signal being received by said second component and causing said second component to read said data from said buffer.

20. A computer system as in claim **9** further comprising:

a bus for carrying a first signal and a second signal, said bus being coupled to said first, second and third components, wherein said first signal is provided by said first component and is synchronized to said second clock, said first signal being received by said second component and said third component and causing said second component to read said data from said buffer, and wherein said second signal is provided by said first component and is synchronized to said third clock, said second signal being received by said third component and by said second component and causing said third component to read said further data from said buffer.

21. A computer system as in claim **19** wherein said data comprises a plurality of words having a selected number of words and wherein said plurality of words are transferred to said buffer without synchronizing any of said plurality of words to any clock except said first clock and wherein said first signal is received by said second component after all of said plurality of words are transferred to said buffer and wherein all of said plurality of words are transferred to said second component from said buffer after said second component receives said first signal.

22. A computer system as in claim **20** wherein said data comprises a plurality of words having a selected number of words, and wherein said plurality of words are transferred to said buffer without synchronizing any of said plurality of words to any clock except said first clock and wherein said first signal is received by said second component after all of said plurality of words are transferred to said buffer, and wherein all of said plurality of words are transferred to said second component from said buffer after said second component receives said first signal, and wherein said further data comprises a further plurality of words, and wherein said further plurality of words are transferred to said buffer without synchronizing any of said further plurality of words to any clock except said first clock and wherein said second signal is received by said third component after all of said further plurality of words are transferred to said buffer and wherein all of said further plurality of words are transferred to said third component from said buffer after said third component receives said second signal.

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